82930A
UNIVERSAL SERIAL BUS MICROCONTROLLER

- **Complete Universal Serial Bus Specification compatibility**
  - **— Supports Isochronous and Non-isochronous data**
  - **— Bi-directional half-duplex link**
- **Serial Bus Interface Engine (SIE)**
  - **— Packet decoding/generation**
  - **— CRC generation and checking**
  - **— NRZI encoding/decoding and bit-stuffing**
- **Four transmit FIFOs**
  - **— Three 16 byte FIFOs**
  - **— One 256 byte FIFO**
- **Four receive FIFOs**
  - **— Three 16 byte FIFOs**
  - **— One 256 byte FIFO**
- **Automatic transmit/receive FIFO management**
- **Four endpoint interrupt vectors**
- **Phase lock loop**
  - **— 12 Mbps or 1.5 Mbps data rate**
- **256 Kbyte External Code/Data memory space**
- **Power-saving Idle and Powerdown Modes**
- **User-selectable Configurations**
  - **— External Wait State**
  - **— Address Range**
  - **— Page Mode**
- **1 Kbyte on-chip data RAM**
- **Four input/output ports**
  - **— 1 open drain port**
  - **— 3 quasi bidirectional ports**
- **Programmable counter array (PCA)**
  - **— 5 capture/compare modules**
- **Industry Standard MCS® 51 UART**
- **Hardware watchdog timer**
- **Three flexible 16-bit timer/counters**
- **Code compatibility with MCS 51 and MCS® 251 microcontrollers**
- **Register-based MCS 251 architecture**
  - **— 40 byte register file**
  - **— Registers accessible as bytes, words, or double words**
- **12 MHz Operation**

Figure 2 is a block diagram showing the 80C251SB microcontroller core and the peripheral USB components combined to comprise the 82930A.The device supports four function endpoints (0–3); endpoint 0 is dedicated to control. The USB device components are: a FIFO memory system with two FIFOs of 256 bytes depth, (one for transmission and one for reception) and six FIFOs of 16 bytes depth (3 for transmission and 3 for reception); a standard serial bus interface unit (SIU); a phase lock loop; and a selectable 12 Mbps or 1.5 Mbps data rate. The 82930A uses the standard instruction set of the MCS 251 architecture.

January 1996 **Order Number: 272797-002**

1.0 BLOCK DIAGRAM

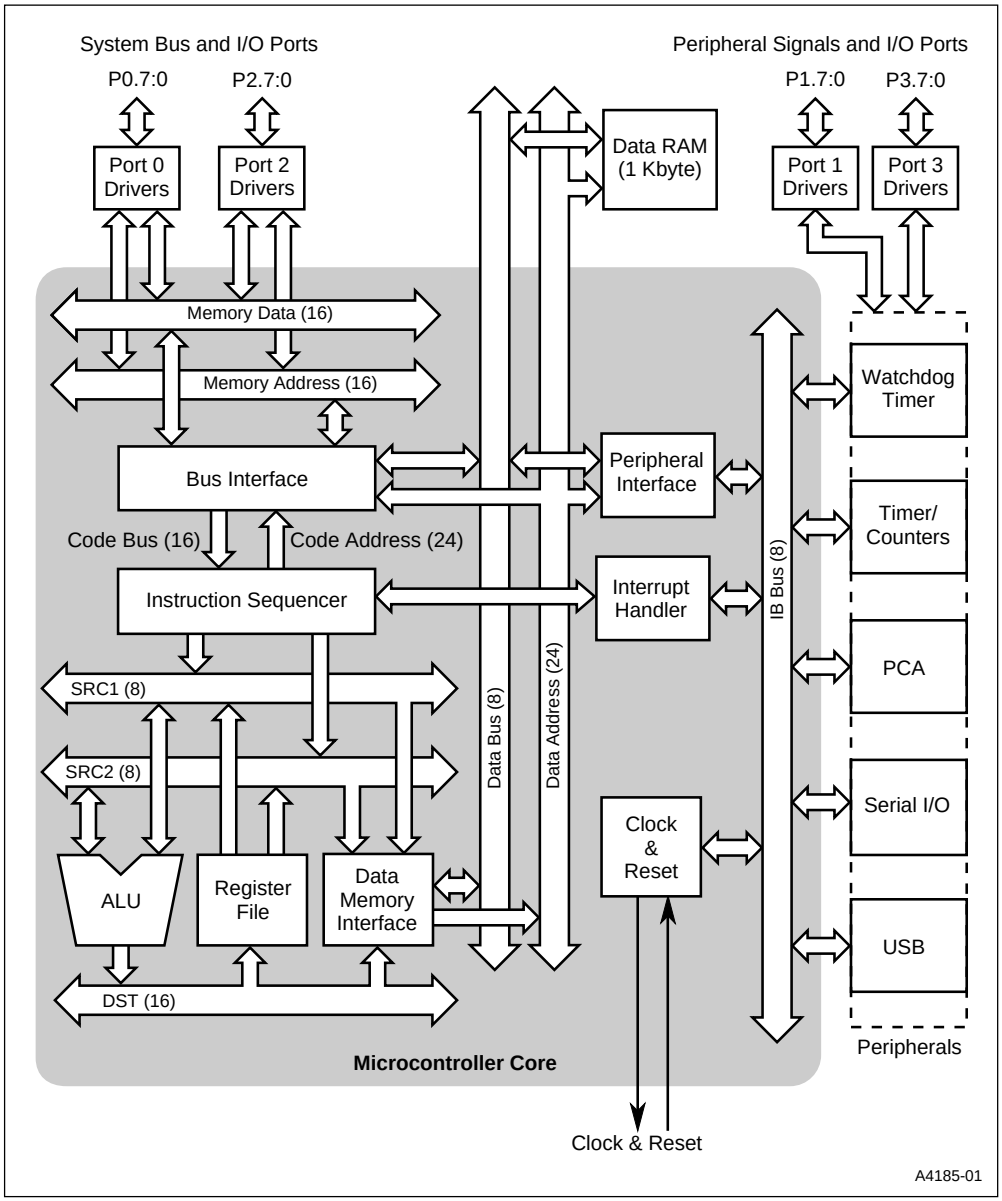


Figure 1. 82930A Block Diagram

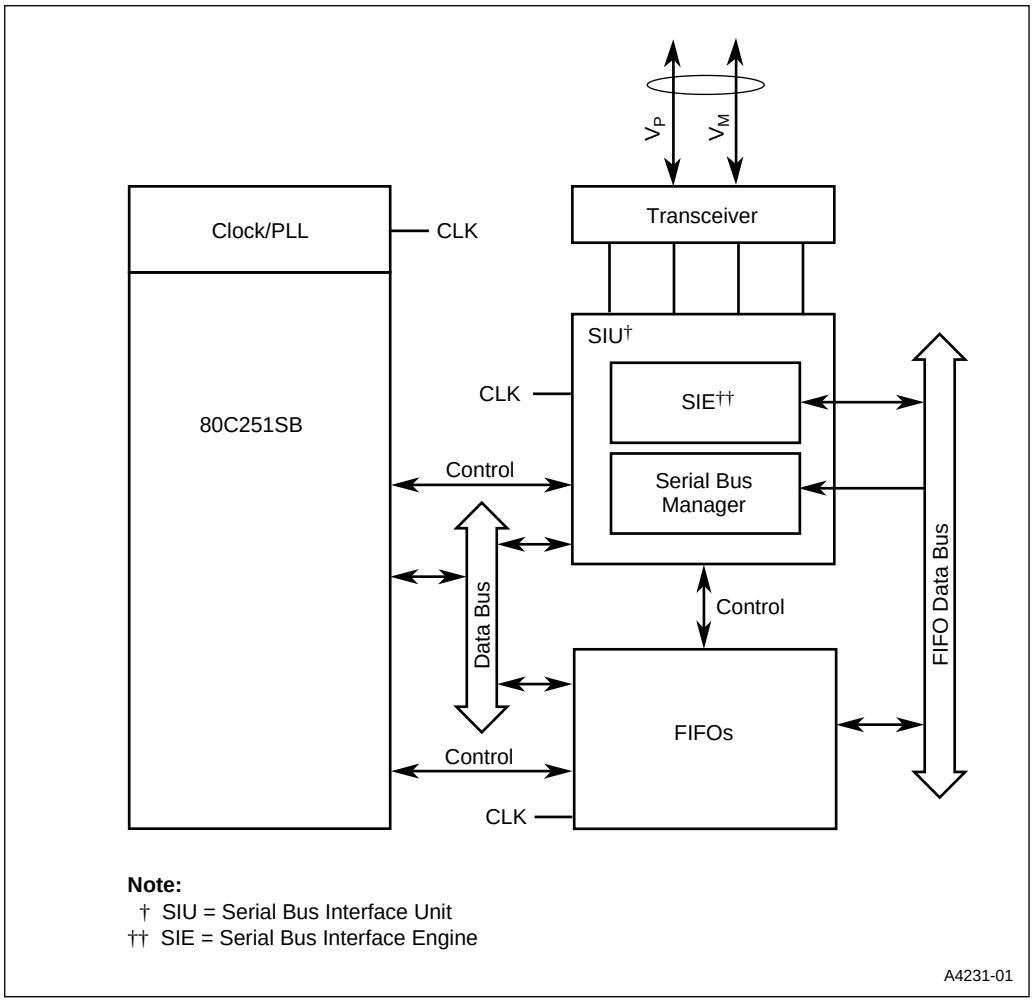


Figure 2. 82930A USB Peripheral Interface

2.0 TEMPERATURE RANGE

The 82930A is tested at room temperature only. Operation beyond room temperature conditions are not tested and are not guaranteed. See Figure 3 for the 82930A marking nomenclature.

3.0 PROCESS INFORMATION

This device is manufactured on a complimentary high-performance metal-oxide semiconductor (CHMOS) process. Additional process and reliability information is available in Intel's *Components Quality and Reliability Handbook* (order number 210997).

4.0 THERMAL CHARACTERISTICS

All thermal impedance data (see Table 1) is approximate for static air conditions at 1 watt of power dissipation. Values change depending on operating conditions and application requirements. The Intel *Packaging Handbook* (order number 240800) describes Intel's thermal impedance test methodology.

Table 1. Thermal Characteristics

Package Type	θ_{JA}	θ_{JC}
68-lead Cerquad	N/A	N/A

5.0 82930A NOMENCLATURE

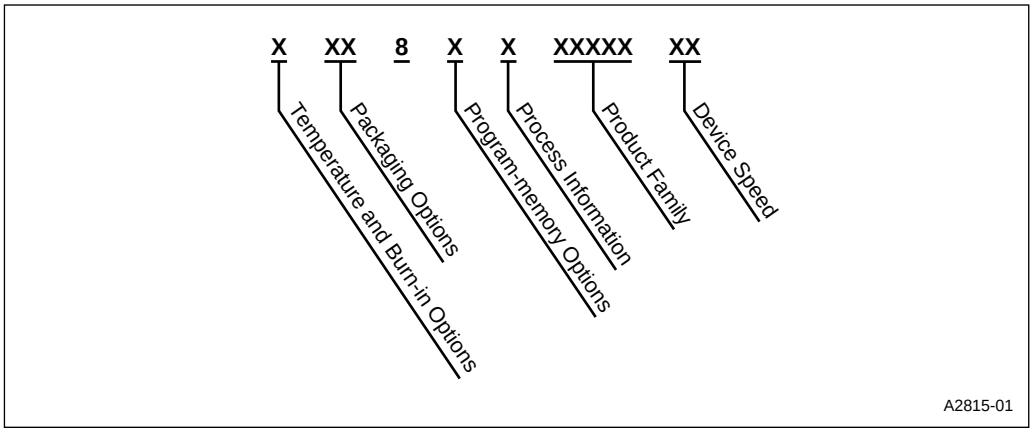


Figure 3. The 82930A Family Nomenclature

Table 2. Description of Product Nomenclature

Parameter	Options	Description
Temperature and Burn-in	no mark	Room Temperature only
Packaging Options	J	Cerquad
Program Memory Options	2	Use external memory
Process Information	no mark	CHMOS
Product Family	930A	Advanced 8-bit microcontroller architecture with on-chip Universal Serial Bus interface (Proof of Concept device)
Device Speed	no mark	12 MHz

6.0 82930A MEMORY MAP

Table 3 contains a description of the 82930A memory map.

Table 3. 82930A Memory Map

Internal Address)	Description	Notes
FF:FFFFH FF:0000H	External Memory: The last 8 bytes of the external address range FF:XFF8H–FF:XFFFH contain Configuration Byte information.	1, 3, 8
FE:FFFFH FE:0000H	External Memory	3
FD:FFFFH FD:0000H	External Memory	3
FC:FFFFH FC:0000H	External Memory	3
FB:FFFFH 04:0000H	Reserved Addresses	4
03:FFFFH 03:0000H	External Memory	3
02:FFFFH 02:0000H	External Memory	3
01:FFFFH 01:0000H	External Memory	3
00:FFFFH 00:0420H	External Memory	5
00:041FH 00:0080H	On-chip RAM	5
00:007FH 00:0020H	On-chip RAM	6
00:001FH 00:0000H	Storage for R0–R7 of Register File	2, 7

NOTES:
1. 18 address lines are bonded out (A15:0, A16:0, or A17:0 selected during chip configuration).
2. The special function registers (SFRs) and the register file have separate internal address spaces.
3. Data in this area is accessible by indirect addressing only.
4. This reserved area returns unspecified values and writes no data.
5. Data is accessible by direct and indirect addressing.
6. Data is accessible by direct, indirect, and bit addressing.
7. Data is accessible by direct, indirect, and register addressing.
8. Eight addresses at the top of all external memory maps are reserved for current and future device Configuration byte information.

7.0 82930A PACKAGE INFORMATION

A diagram of the 82930A cerquad package is illustrated in Figure 4. Indexes of the lead arrangements are contained in Table 4 and Table 5. The signal descriptions for all leads are located in Table 6.

NOTE: Reserved leads must be left unconnected.

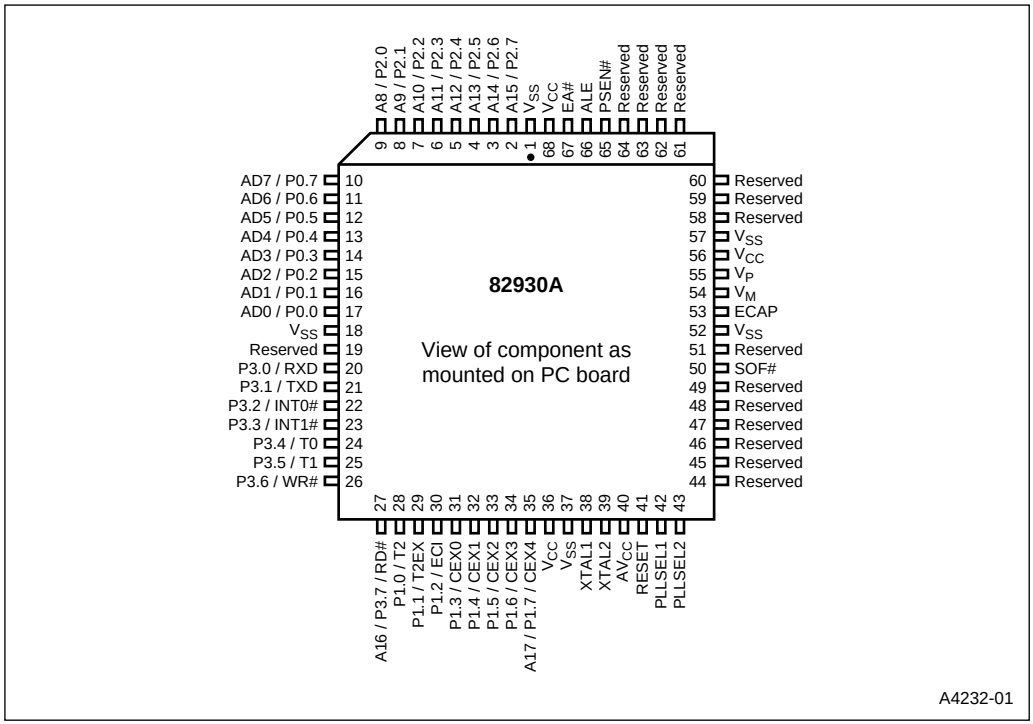


Figure 4. 82930A 68-lead Cerquad

Table 4. 68-lead Cerquad Signal Assignment Arranged by Functional Categories

Address & Data	
Name	**Lead**
AD0/P0.0	17
AD1/P0.1	16
AD2/P0.2	15
AD3/P0.3	14
AD4/P0.4	13
AD5/P0.5	12
AD6/P0.6	11
AD7/P0.7	10
A8/P2.0	9
A9/P2.1	8
A10/P2.2	7
A11/P2.3	6
A12/P2.4	5
A13/P2.5	4
A14/P2.6	3
A15/P2.7	2
P3.7/RD#/A16	27
P1.7/CEX4/A17	35

Input/Output	
Name	**Lead**
P1.0/T2	28
P1.1/T2EX	29
P1.2/ECI	30
P1.3/CEX0	31
P1.4/CEX1	32
P1.5/CEX2	33
P1.6/CEX3	34
P1.7/CEX4/A17	35
P3.0/RXD	20
P3.1/TXD	21
P3.4/T0	24
P3.5/T1	25

Bus Control & Status	
Name	**Lead**
P3.6/WR#	26
P3.7/RD#/A16	27
ALE	66
PSEN#	65

Power & Ground	
Name	**Lead**
V_{CC}	36, 56, 68
AV_{CC}	40
EA#	67
V_{SS}	1, 18, 37, 52, 57

USB	
Name	**Lead**
PLLSEL1	42
PLLSEL2	43
SOF#	50
ECAP	53
VM	54
VP	55

Processor Control	
Name	**Lead**
P3.2/INT0#	22
P3.3/INT1#	23
EA#	67
RST	41
XTAL1	38
XTAL2	39

Table 5. 68-lead Cerquad Signal Assignment Arranged by Number

Lead Number	Name
1	V_{SS}
2	A15/P2.7
3	A14/P2.6
4	A13/P2.5
5	A12/P2.4
6	A11/P2.3
7	A10/P2.2
8	A9/P2.1
9	A8/P2.0
10	AD7/P0.7
11	AD6/P0.6
12	AD5/P0.5
13	AD4/P0.4
14	AD3/P0.3
15	AD2/P0.2
16	AD1/P0.1
17	AD0/P0.0
18	V_{SS}
19	Reserved
20	P3.0/RXD
21	P3.1/TXD
22	P3.2/INT0#
23	P3.3/INT1#

Lead Number	Name
24	P3.4/T0
25	P3.5/T1
26	P3.6/WR#
27	A16/P3.7/RD#
28	P1.0/T2
29	P1.1/T2EX
30	P1.2/ECI
31	P1.3/CEX0
32	P1.4/CEX1
33	P1.5/CEX2
34	P1.6/CEX3
35	A17/P1.7/CEX4
36	V_{CC}
37	V_{SS}
38	XTAL1
39	XTAL2
40	AV_{CC}
41	RST
42	PLLSEL1
43	PLLSEL2
44	Reserved
45	Reserved
46	Reserved

Lead Number	Name
47	Reserved
48	Reserved
49	Reserved
50	SOF#
51	Reserved
52	V_{SS}
53	ECAP
54	VM
55	VP
56	V_{CC}
57	V_{SS}
58	Reserved
59	Reserved
60	Reserved
61	Reserved
62	Reserved
63	Reserved
64	Reserved
65	PSEN#
66	ALE
67	EA#
68	V_{CC}

8.0 SIGNAL DESCRIPTIONS

Table 6. Signal Descriptions

Signal Name	Type	Description	Multi-plexed With
A17	O	**18th Address Bit (A17).** Output to memory as 18th external address bit (A17) in extended bus applications, depending on the values of bits RD0 and RD1 in configuration byte UCONFIG0 (see Table 7). See also RD#, PSEN#:	P1.7/CEX4
A16	O	**Address Line 16**. See RD#.	RD#
A15:8†	O	**Address Lines**. Upper address lines for the external bus.	P2.7:0
AD7:0†	I/O	**Address/Data Lines**. Multiplexed lower address lines and data lines for external memory.	P0.7:0
ALE	O	**Address Latch Enable**. ALE signals the start of an external bus cycle and indicates that valid address information is available on lines A15:8 and AD7:0. An external latch can use ALE to demultiplex the address from the address/data bus.	PROG#
AV_{CC}	PWR	**Analog V_{CC}**. A separate V_{CC} input for the phase locked loop circuitry.	
CEX4:0	I/O	**Programmable Counter Array (PCA) Input/Output Leads**. These are input signals for the PCA capture mode and output signals for the PCA compare mode and PCA PWM mode.	P1.6:3 P1.7/A17
EA#	I	**External Access**. Must be externally connected to V_{SS} in order to direct program memory accesses off-chip.	
ECAP	I	**External Capacitor**. Must be connected to a 0.1µF capacitor (or larger) to ensure proper operation of the differential line driver. The other lead of the capacitor must be connected to V_{SS}.	
ECI	I	**PCA External Clock Input**. External clock input to the 16-bit PCA timer.	P1.2
INT1:0#	I	**External Interrupts 0 and 1**. These inputs set bits IE1:0 in the TCON register. If bits IT1:0 in the TCON register are set, bits IE1:0 are set by a falling edge on INT1#/INT0#. If bits INT1:0 are clear, bits IE1:0 are set by a low level on INT1:0#.	P3.3:2
P0.7:0	I/O	**Port 0**. This is an 8-bit, open-drain, bidirectional I/O port.	AD7:0
P1.0 P1.1 P1.2 P1.7:3	I/O	**Port 1**. This is an 8-bit, bidirectional I/O port with internal pullups.	T2 T2EX ECI CEX3:0 CEX4/A17
P2.7:0	I/O	**Port 2**. This is an 8-bit, bidirectional I/O port with internal pullups.	A15:8
P3.0 P3.1 P3.3:2 P3.5:4 P3.6 P3.7	I/O	**Port 3**. This is an 8-bit, bidirectional I/O port with internal pullups.	RXD TXD INT1:0# T1:0 WR# RD#/A16

† The descriptions of A15:8/P2.7:0 and AD7:0/P0.7:0 are for the nonpage-mode chip configuration. If the chip is configured for page-mode operation, port 0 carries the lower address bits (A7:0), and port 2 carries the upper address bits (A15:8) and the data (D7:0).

Table 6. Signal Descriptions (Continued)

Signal Name	Type	Description	Multi-plexed With
PLLSEL1	I	**Phase Locked Loop (Select 1)**. Selects data rate (see Table 8)	—
PLLSEL2	I	**Phase Locked Loop (Select 2)**. Selects data rate (see Table 8)	—
PSEN#	O	**Program Store Enable**. Read signal output. This output is asserted for a memory address range that depends on bits RD0 and RD1 in configuration byte UCONFIG0 (see RD# and Table 7):	—
RD#	O	**Read or 17th Address Bit (A16).** Read signal output to external data memory or 17th external address bit (A16), depending on the values of bits RD0 and RD1 in configuration byte UCONFIG0. (See PSEN# and Table 7):	P3.7/A16
RST	I	**Reset**. Reset input to the chip. Holding this lead high for 64 oscillator periods while the oscillator is running resets the device. The port leads are driven to their reset conditions when a voltage greater than V_{IH1} is applied, whether or not the oscillator is running. This lead has an internal pulldown resistor, which allows the device to be reset by connecting a capacitor between this lead and V_{CC}. Asserting RST when the chip is in idle mode or powerdown mode returns the chip to normal operation.	—
RXD	I/O	**Receive Serial Data**. RXD sends and receives data in serial I/O mode 0 and receives data in serial I/O modes 1, 2, and 3.	P3.0
SOF#	O	**Start of Frame**. This lead is asserted for eight states when an SOF token is received.	—
T1:0	I	**Timer 1:0 External Clock Inputs**. When timer 1:0 operates as a counter, a falling edge on the T1:0 lead increments the count.	P3.5:4
T2	I/O	**Timer 2 Clock Input/Output**. For the timer 2 capture mode, this signal is the external clock input. For the clock-out mode, it is the timer 2 clock output.	P1.0
T2EX	I	**Timer 2 External Input**. In timer 2 capture mode, a falling edge initiates a capture of the timer 2 registers. In auto-reload mode, a falling edge causes the timer 2 registers to be reloaded. In the up-down counter mode, this signal determines the count direction: 1 = up, 0 = down.	P1.1
TXD	O	**Transmit Serial Data**. TXD outputs the shift clock in serial I/O mode 0 and transmits serial data in serial I/O modes 1, 2, and 3.	P3.1
V_{CC}	PWR	**Supply Voltage**. Connect this lead to the +5V supply voltage.	—
V_P	I/O	**Voltage Plus**. USB plus voltage line interface.	—
V_M	I/O	**Voltage Minus**. USB minus voltage line interface.	—
V_{SS}	GND	**Circuit Ground**. Connect this lead to ground.	—
WR#	O	**Write**. Write signal output to external memory.	P3.6

† The descriptions of A15:8/P2.7:0 and AD7:0/P0.7:0 are for the nonpage-mode chip configuration. If the chip is configured for page-mode operation, port 0 carries the lower address bits (A7:0), and port 2 carries the upper address bits (A15:8) and the data (D7:0).

Table 6. Signal Descriptions (Continued)

Signal Name	Type	Description	Multi-plexed With
XTAL1	I	**Input to the On-chip, Inverting, Oscillator Amplifier**. To use the internal oscillator, a crystal/resonator circuit is connected to this lead. If an external oscillator is used, its output is connected to this lead. XTAL1 is the clock source for internal timing.	—
XTAL2	O	**Output of the On-chip, Inverting, Oscillator Amplifier**. To use the internal oscillator, a crystal/resonator circuit is connected to this lead. If an external oscillator is used, leave XTAL2 unconnected.	—

† The descriptions of A15:8/P2.7:0 and AD7:0/P0.7:0 are for the nonpage-mode chip configuration. If the chip is configured for page-mode operation, port 0 carries the lower address bits (A7:0), and port 2 carries the upper address bits (A15:8) and the data (D7:0).

Table 7. Memory Signal Selections (RD1:0)

RD1:0	P1.7/CEX/ A17	RD#	PSEN#	WR#	Features
0 0	A17	RD# = A16	Asserted for all addresses	Asserted for writes to all memory locations	256-Kbyte external memory
0 1	P1.7/CEX4	RD# = A16	Asserted for all addresses	Asserted for writes to all memory locations	128-Kbyte external memory
1 0	P1.7/CEX4	P3.7 only	Asserted for all addresses	Asserted for writes to all memory locations	One additional port lead
1 1	P1.7/CEX4	Asserted for ≤ 7F:FFFFH	Asserted for ≥ 80:0000H	Asserted for all compatible MCS 51 memory locations	Compatible with MCS 51 microcontrollers

Table 8. 82930A Operating Frequency

PLLSEL2 Lead 43	PLLSEL1 Lead 42	USB Rate	Internal 82930A Clock Frequency	External (XTAL1) Frequency Required
0	0	N/A	N/A	N/A
0	1	N/A	N/A	N/A
1	0	1.5 Mbps	6 Mhz	12 Mhz
1	1	12 Mbps	12 Mhz	12 Mhz

9.0 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS†

Ambient Temperature under Bias..... 0°C to +70°C
Storage Temperature ..... -65°C to +150°C
Voltage on EA#/VPP Lead to Vss ..... 0 V to +13.0 V
Voltage on Any other Lead to Vss..... -0.5 V to +6.5 V
Iol per I/O Lead ..... 15 mA
Power Dissipation ..... 1.5 W

NOTE: Maximum power dissipation is based on package heat-transfer limitations, not device power consumption.

OPERATING CONDITIONS†

T_A (Ambient Temperature Under Bias):
Commercial ..... Room temperature only
V_{CC} (Digital Supply Voltage) ..... 4.5 V to 5.5 V
V_{SS} ..... 0 V

NOTICE: This document contains information on products in the design phase of development. Do not finalize a design with this information. Revised information will be published when the product is available. Verify with your local Intel Sales Office that you have the latest datasheet before finalizing a design.

†**WARNING:** *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

9.1 DC Characteristics

Table 9 describes the 82930A D.C. Characteristics.

Table 9. DC Characteristics at Operating Conditions

Sym-bol	Parameter	Min	Typical (1)	Max	Units	Test Conditions
V_{IL}	Input Low Voltage (except EA#)	-0.5		0.2Vcc-0.1	V	
V_{IL1}	Input Low Voltage (EA#)	0		0.2VCC-0.3	V	
V_{IH}	Input High Voltage (except XTAL1, RST)	0.2VCC+0.9		VCC+0.5	V	
V_{IH1}	Input High Voltage (XTAL1, RST)	0.7VCC		VCC+0.5	V	
V_{OL}	Output Low Voltage (Port 1, 2, 3)			0.3 0.45 1.0	V	IOL=100uA (note 2,3) IOL=1.6mA IOL=3.5mA
V_{OL1}	Output Low Voltage (Port 0, ALE, PSEN#, SOF#)			0.3 0.45 1.0	V	IOL=200uA (note 2,3) IOL=3.2mA IOL=7.0mA
V_{OH}	Output High Voltage (port 1, 2, 3,ALE, PSEN#, SOF#)	VCC-0.3 VCC-0.7 VCC-1.5			V	IOH=-10uA (note 4) IOH=-30uA IOH=-60uA

NOTES:

1. Typical values are obtained using V_{CC}=5.0V, TA=25 C and are not guaranteed.
2. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follow:
   Maximum I_{OL} per Port Lead:10mA
   Maximum I_{OL} per 8-bit Port-
   Port 0:26mA
   Ports 1-3:15mA
   Maximum Total I_{OL} for all
   Output Leads:71mA
   If I_{OL} exceeds the test conditions, V_{OL} may exceed the related specification. Leads are not guaranteed to sink current greater than the listed test conditions.
3. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses above 0.4V on the low level outputs of ALE and Ports 1, 2 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 leads when these leads change from 1 to 0. In applications where capacitive loading exceeds 100pF, the noise pulses on these signals may exceed 0.8V. It may be desirable to qualify ALE or other signals with a Schmitt Trigger, or CMOS-level input logic.
4. Capacitive loading on Ports 0 and 2 cause the V_{OH} on ALE and PSEN to drop below the 0.9 V_{CC} specification when the address lines are stabilizing.
5. The abbreviations ‘LS’ and ‘FS’ indicate ‘Low Speed’ and ‘Full Speed’ respectively.

Table 9. DC Characteristics at Operating Conditions

Sym-bol	Parameter	Min	Typical (1)	Max	Units	Test Conditions
V_{OH1}	Output High Voltage (Port 0 in External Address)	VCC-0.3 VCC-0.7 VCC-1.5			V	IOH=-200uA (note 4) IOH=-3.2mA IOH=-7.0mA
I_{IL}	Logical 0 Input Current (Port 1,2,3)			-50	uA	VIN=0.45V
I_{LI}	Input Leakage Current (Port 0)			+/- 10	uA	0.45<VIN<VCC
I_{TL}	Logical 1-to-0 Transition Current (Port 1, 2,3)			-650	uA	VIN=2.0V
R_{RST}	RST Pulldown Resistor	40		225	kohm	
I_{PD}	Power Down Current		10	50	uA	
I_{DL}	Idle Mode Icc-LS (Note 5) Idle Mode Icc-FS		5	10 20	mA	Xtal1=12MHz
I_{CC}	Active Icc-LS (Note 5) Active Icc-FS		15	50 100	mA	Xtal1=12MHz

NOTES:

1. Typical values are obtained using V_{CC}=5.0V, TA=25 C and are not guaranteed.
2. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follow:
   Maximum I_{OL} per Port Lead:10mA
   Maximum I_{OL} per 8-bit Port-
   Port 0:26mA
   Ports 1-3:15mA
   Maximum Total I_{OL} for all
   Output Leads:71mA
   If I_{OL} exceeds the test conditions, V_{OL} may exceed the related specification. Leads are not guaranteed to sink current greater than the listed test conditions.
3. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses above 0.4V on the low level outputs of ALE and Ports 1, 2 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 leads when these leads change from 1 to 0. In applications where capacitive loading exceeds 100pF, the noise pulses on these signals may exceed 0.8V. It may be desirable to qualify ALE or other signals with a Schmitt Trigger, or CMOS-level input logic.
4. Capacitive loading on Ports 0 and 2 cause the V_{OH} on ALE and PSEN to drop below the 0.9 V_{CC} specification when the address lines are stabilizing.
5. The abbreviations ‘LS’ and ‘FS’ indicate ‘Low Speed’ and ‘Full Speed’ respectively.

9.2 AC Characteristics

Table 10 lists AC timing parameters for the 82930A.

NOTE: Test Conditions:
Capacitive load on all leads = 50pF
Rise and Fall times = 10ns
Fosc = 12MHz

Table 10. AC Characteristics at Operating Conditions

Symbol	Parameter (6)	@ 12MHz	F_{osc} Variable		Units
			Min	Max	
FOSC	XTAL1 Frequency	12	11.970	12.030	MHz
TOSC	$1/F_{OSC}$	83.33	83.54	83.13	ns
TLHLL	ALE Pulse Width 82930A-LS 82930A-FS	76.3 34.6	$T_{OSC} - 7$ $0.5T_{OSC} - 7$		ns (3)
TAVLL	Address Valid to ALE Low 82930A-LS 82930A-FS	70.3 28.6	$T_{OSC} - 13$ $0.5T_{OSC} - 13$		ns (3)
TLLAX	Address Hold after ALE Low 82930A-LS 82930A-FS	10 10	10 10		ns
TRLRH (2)	RD# or PSEN# Pulse Width 82930A-LS 82930A-FS	156.6 73.3	$2T_{OSC} - 10$ $T_{OSC} - 10$		ns (4)
TWLWH	WR# Pulse Width 82930A-LS 82930A-FS	156.6 73.3	$2T_{OSC} - 10$ $T_{OSC} - 10$		ns (4)
TLHRL (2)	ALE High to RD# or PSEN# Low 82930A-LS 82930A-FS	70.3 28.6	$T_{OSC} - 13$ $0.5T_{OSC} - 13$		ns
TLHAX	ALE High to Address Hold 82930A-LS 82930A-FS	70.3 28.6	$T_{OSC} - 13$ $0.5T_{OSC} - 13$		ns (3)

NOTE:
1. 12 MHz +- 0.25%.
2. Specifications for PSEN# are identical to those for RD#.
3. If a wait state is added by extending ALE, add $2T_{OSC}$ for 82930A-LS and T_{OSC} for 82930A-FS.
4. If a wait state is added by extending RD#/PSEN#/WR#, add $2T_{OSC}$ for 82930A-LS and T_{OSC} for 82930A-FS.
5. If wait states are added as described in both Note (4) and Note (3), add a total of $4T_{OSC}$ for 82930A-LS and $2T_{OSC}$ for 82930A-FS.
6. The abbreviations ‘LS’ and ‘FS’ indicate ‘Low Speed’ and ‘Full Speed’ respectively.

Table 10. AC Characteristics at Operating Conditions

Symbol	Parameter (6)	@ 12MHz	F_{osc} Variable		Units
			Min	Max	
T_{RLDV} (2)	RD# or PSEN# Low to Valid Data/Instruct. In 82930A-LS 82930A-FS	 133.6 50.3		 2Tosc – 33 Tosc – 33	ns (4)
T_{RHDX} (2)	Data/Instruct. Hold After RD# or PSEN# High	0	0		ns
T_{RLAZ} (2)	RD# or PSEN# Low to Address Float	0		0	ns
T_{RHDZ} (2)	Data/Instruct. Float After RD# or PSEN# High 82930A-LS 82930A-FS	 70.3 28.6		 T_{OSC} – 13 $0.5T_{OSC}$ – 13	ns
T_{RHLH}	RD# High to ALE High 82930A-LS 82930A-FS	 239.9 114.9	 $2T_{OSC}$ +10 T_{OSC} +10		ns
T_{PHLH}	PSEN# High to ALE High 82930A-LS 82930A-FS	 73.3 31.6	 T_{osc} - 10 $0.5T_{osc}$ - 10		
T_{WHLH}	WR# High to ALE High 82930A-LS 82930A-FS	 239.9 114.9	 $2T_{OSC}$ +10 T_{OSC} +10		ns
T_{AVDV1}	Address (P0) Valid to Valid Data/Instruction In 82930A-LS (3) 82930A-FS (3)	 222.9 97.9		 $3T_{OSC}$ – 27 $1.5T_{OSC}$ – 27	ns (3,4,5)
T_{AVDV2}	Address (P2) Valid to Valid Data/Instruction In 82930A-LS (3) 82930A-FS (3)	 222.9 97.9		 $3T_{OSC}$ – 27 $1.5T_{OSC}$ – 27	ns (3,4,5)
T_{AVDV3}	Address (P0) Valid to Valid Instruction In 82930A-LS 82930A-FS	 222.9 97.9		 $3T_{OSC}$ – 27 $1.5T_{OSC}$ – 27	ns

NOTE:
1. 12 MHz +- 0.25%.
2. Specifications for PSEN# are identical to those for RD#.
3. If a wait state is added by extending ALE, add $2T_{OSC}$ for 82930A-LS and T_{OSC} for 82930A-FS.
4. If a wait state is added by extending RD#/PSEN#/WR#, add $2T_{OSC}$ for 82930A-LS and T_{OSC} for 82930A-FS.
5. If wait states are added as described in both Note (4) and Note (3), add a total of $4T_{OSC}$ for 82930A-LS and $2T_{OSC}$ for 82930A-FS.
6. The abbreviations ‘LS’ and ‘FS’ indicate ‘Low Speed’ and ‘Full Speed’ respectively.

Table 10. AC Characteristics at Operating Conditions

Symbol	Parameter (6)	@ 12MHz	F_{osc} Variable		Units
			Min	Max	
T_{AVRL} (2)	Address Valid to RD# or PSEN# 82930A-LS 82930A-FS	 73.3 31.6	 T_{OSC}– 10 $0.5T_{OSC}$ – 10		ns (3)
T_{AVWL1}	Address (P0) Valid to WR# Low 82930A-LS 82930A-FS	 73.3 31.6	 T_{OSC} – 10 $0.5T_{OSC}$ – 10		ns (3)
T_{AVWL2}	Address (P2) Valid to WR# Low 82930A-LS 82930A-FS	 63.3 21.6	 T_{OSC} – 20 $0.5T_{OSC}$ – 20		ns (3)
T_{WHQX}	Data Hold after WR# High 82930A-LS 82930A-FS	 70.3 28.6	 T_{OSC} – 13 $0.5T_{OSC}$ – 13		ns
T_{QVWH}	Data Valid to WR# High 82930A-LS 82930A-FS	 151.6 68.3	 $2T_{OSC}$ – 15 T_{OSC} – 15		ns (4)
T_{WHAX}	WR# High to Address Hold 82930A-LS 82930A-FS	 236.9 111.9	 $2T_{OSC}$ – 13 T_{OSC} – 13		ns

NOTE:
1. 12 MHz +- 0.25%.
2. Specifications for PSEN# are identical to those for RD#.
3. If a wait state is added by extending ALE, add $2T_{OSC}$ for 82930A-LS and T_{OSC} for 82930A-FS.
4. If a wait state is added by extending RD#/PSEN#/WR#, add $2T_{OSC}$ for 82930A-LS and T_{OSC} for 82930A-FS.
5. If wait states are added as described in both Note (4) and Note (3), add a total of $4T_{OSC}$ for 82930A-LS and $2T_{OSC}$ for 82930A-FS.
6. The abbreviations ‘LS’ and ‘FS’ indicate ‘Low Speed’ and ‘Full Speed’ respectively.

9.2.1 SYSTEM BUS TIMINGS

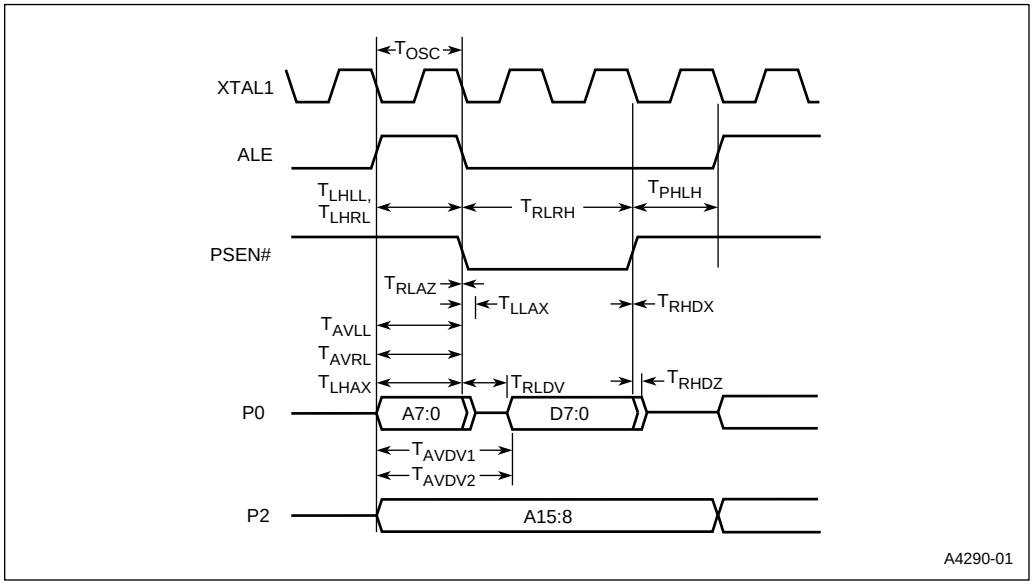


Figure 5. 82930A Instruction Read, Non-page Mode

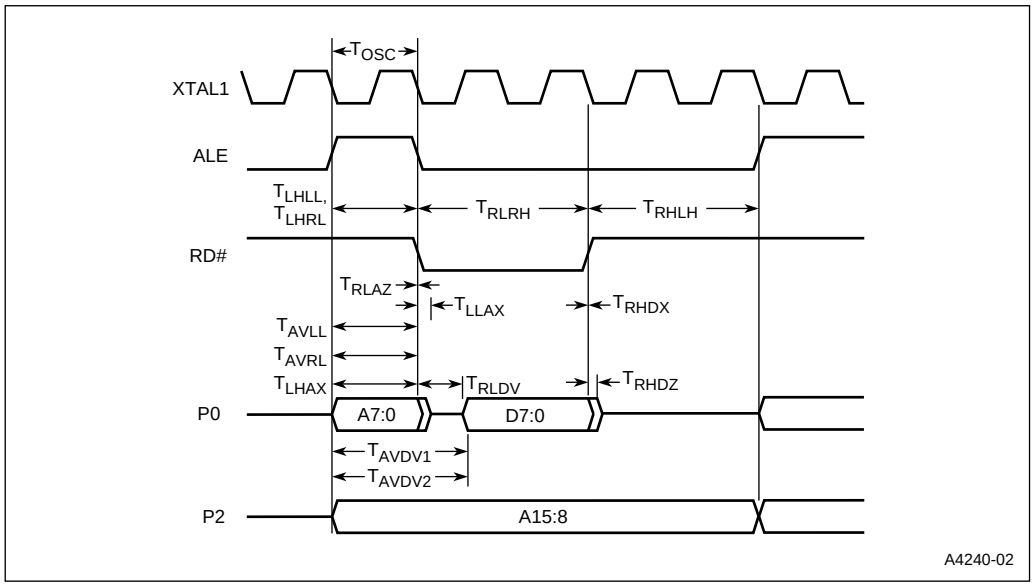


Figure 6. 82930A Data Read, Non-page Mode

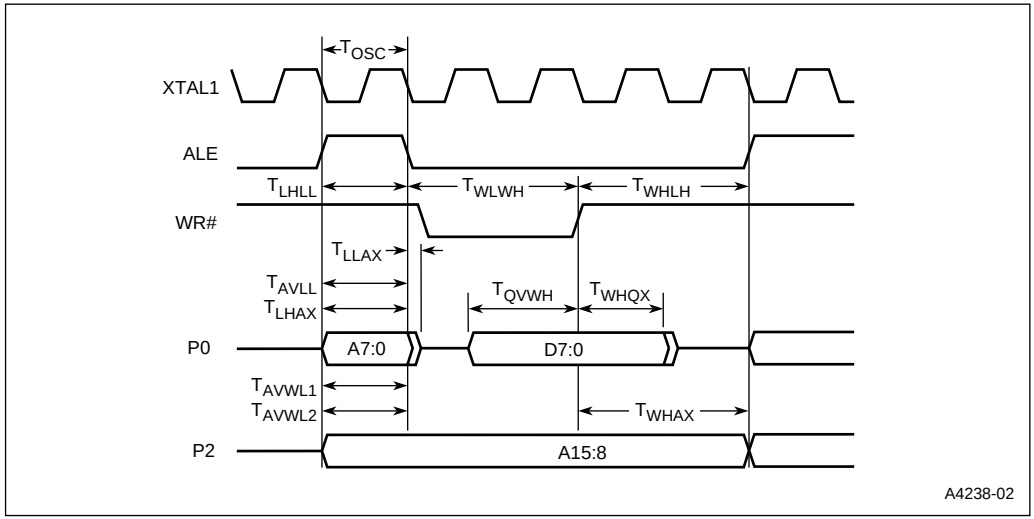


Figure 7. 82930A Data Write, Non-page Mode

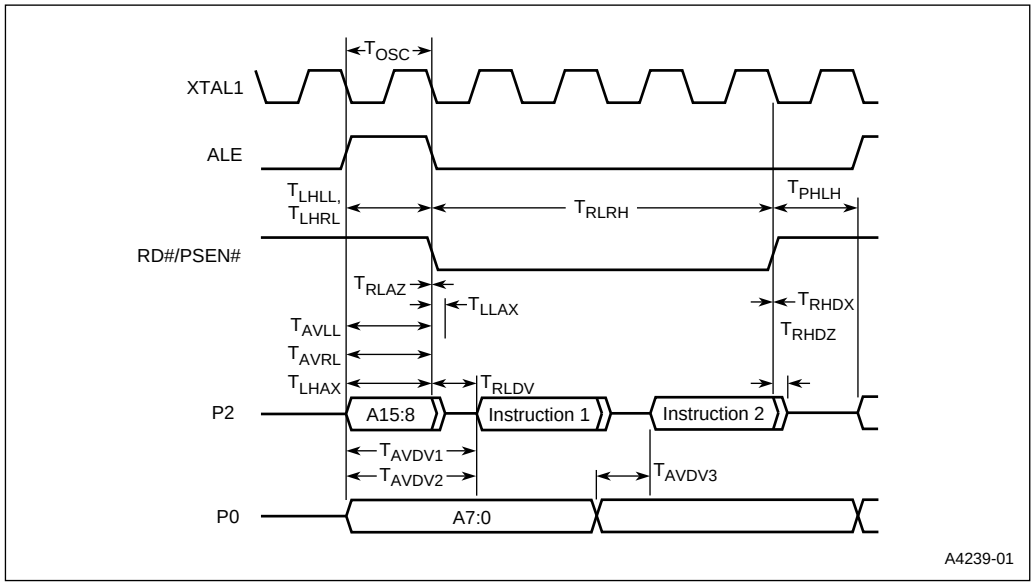


Figure 8. 82930A Instruction Read, Page Mode

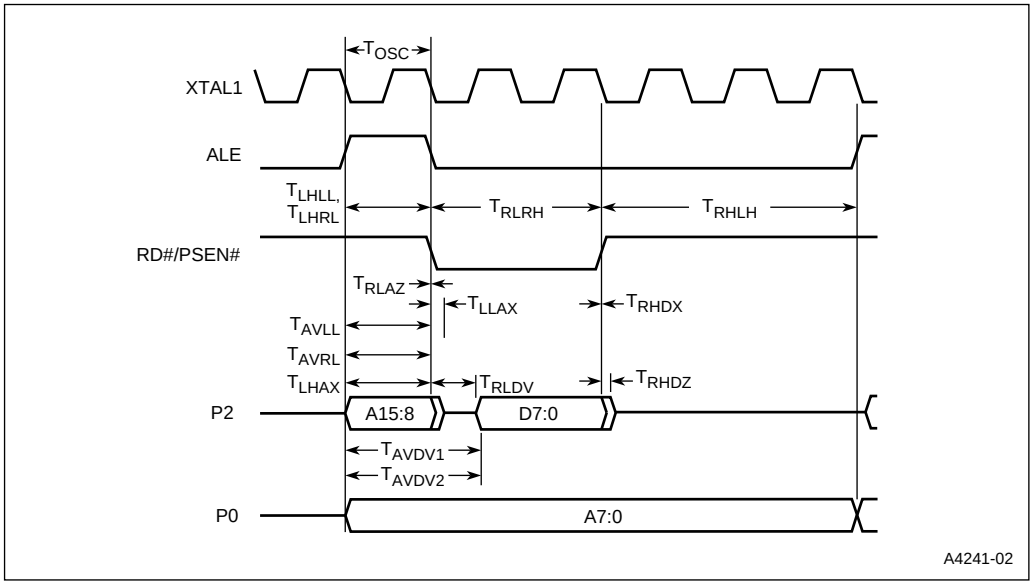


Figure 9. 82930A Data Read, Page Mode

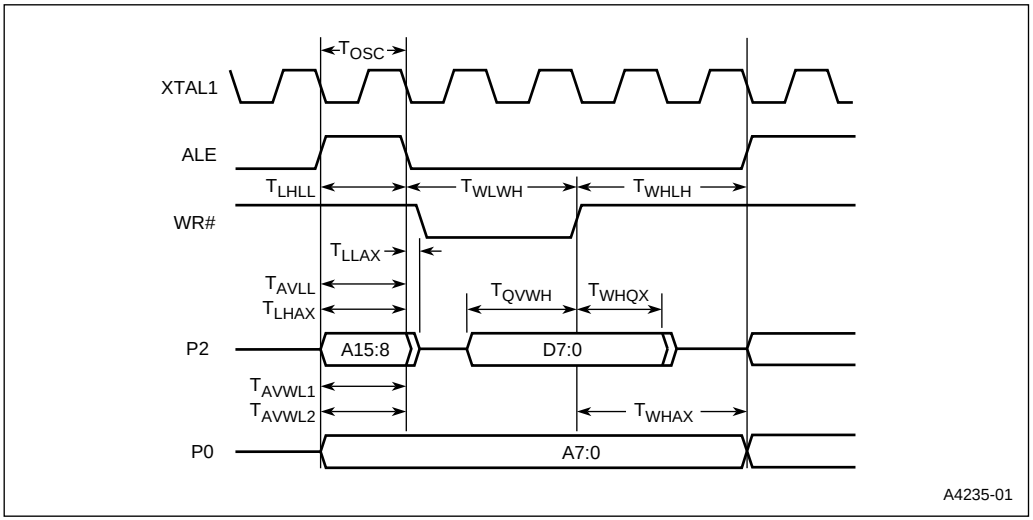


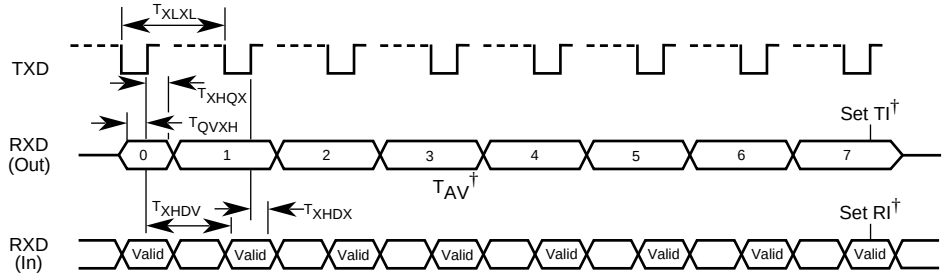
Figure 10. 82930A Data write, Page Mode

9.3 Serial Port Shift Register Mode

Table 11 contains the specifications for the serial port in shift register mode. Figure 11 illustrates this timing.

Table 11. Serial Port Timing — Shift Register Mode

Sym-bol	Parameter	Min	Max	Units
T_{XLXL}	Serial Port Clock Cycle Time	$12T_{OSC}$		ns
T_{QVSH}	Output Data Setup to Clock Rising Edge	$10T_{OSC} - 133$		ns
T_{XHQX}	Output Data hold after Clock Rising Edge	$2T_{OSC} - 117$		ns
T_{XHDX}	Input Data Hold after Clock Rising Edge	0		ns
T_{XHDV}	Clock Rising Edge to Input Data Valid		$10T_{OSC} - 133$	ns

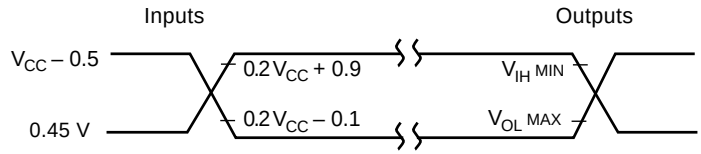


†TI and RI are set during S1P1 of the peripheral cycle following the shift of the eighth bit.

A2592-02

Figure 11. Serial Port Waveform — Shift Register Mode

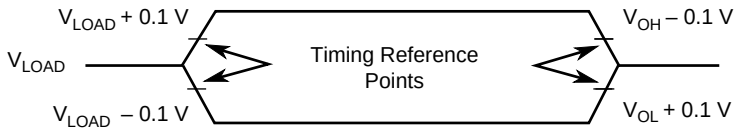
9.4 Testing Waveforms



AC inputs during testing are driven at V_{CC} – 0.5V for a logic 1 and 0.45 V for a logic 0. Timing measurements are made at a min of V_{IH} for a logic 1 and V_{OL} for a logic 0.

A4118-01

Figure 12. A.C. Testing Input, Output Waveforms



For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loading V_{OH}/V_{OL} level occurs with I_{OL}/I_{OH} = ± 20 mA.

A4117-01

Figure 13. Float Waveforms

10.0 CONFIGURATION REGISTERS

The following two sections detail the user configuration registers.

10.1 UCONFIG0

UCONFIG0 Address FF:FFF8H†

7							0
—	WSA1#	WSA0#	XALE#	RD1	RD0	PAGE#	SRC

Bit Number	Bit Mnemonic	Function
7	—	Reserved. Set this bit.
6:5	WSA1#, WSA0#	Wait State Select (for all pages except 01:XXXXH). WSA1# WSA0# Description 1 1 No wait states 1 0 Insert 1 state for all pages except the 01: page 0 1 Insert 2 states for all pages except the 01: page 0 0 Insert 3 states for all pages except the 01: page
4	XALE#	Extend ALE: If this bit is set, the time of the ALE pulse is T_{OSC}. Clearing this bit extends the time of the ALE pulse from T_{OSC} to $3T_{OSC}$, which adds one external wait state.
3:2	RD1, RD0	RD# and PSEN# function select: RD1 RD0 RD# Range P1.7/CEX4/A17 PSEN# Range 0 0 RD# = A16 A17only All Addresses 0 1 RD# = A16 P1.7/CEX4 All Addresses 1 0 P3.7 only P1.7/CEX4 All Addresses 1 1 ≤ 7F:FFFFH P1.7/CEX4 ≥ 80:0000H
1	PAGE#	Page Mode Select: Clear this bit for page-mode (A15:8/D7:0 on P2, and A7:0 on P0). Set this bit for nonpage-mode (A15:8 on P2, and A7:0/D7:0 on P0 (compatible with MCS 51 microcontrollers)).
0	SRC	Source Mode/Binary Mode Select: Set this bit for source mode. Clear this bit for binary mode (binary-code compatible with MCS 51 microcontrollers).

†82930A devices must have EA# connected to V_{SS} and fetch configuration byte information from external application memory based on an internal address range of FF:FFF9:8H.

Figure 14. External Memory User Configuration Byte 0

10.2 UCONFIG1

UCONFIG1 Address FF:FFF9H†

7							0
—	—	—	INTR	—	WSB1#	WSB0#	—

Bit Number	Bit Mnemonic	Function
7:5	—	Reserved; set these bits.
4	INTR	Interrupt Mode: If this bit is set, interrupts push 4 bytes onto the stack (the 3 bytes of the PC register and the PSW1 register). If this byte is clear, interrupts push 2 bytes onto the stack (the 2 lower bytes of the PC register).
3	—	Reserved. Set this bit.
2:1	WSB1# WSB0#	Wait States (01:XXXXH page only) WSB1# WSB0# Description 1 1 No wait states 1 0 Insert 1 wait state for the 01: page 0 1 Insert 2 wait states for the 01: page 0 0 Insert 3 wait states for the 01: page
0	—	Reserved. Set this bit.

†82930A devices must have EA# connected to V_{SS} and fetch configuration byte information from external application memory based on an internal address range of FF:FFF9:8H.

Figure 15. External Memory User Configuration Byte 1

11.0 USB ELECTRICAL SPECIFICATIONS

11.1 Signaling Levels

Table 12 is a summary of the USB specification signaling levels. Selected signaling levels are described in the following sections.

Table 12. USB Signaling Levels

Bus State	Signaling Levels	
	From Originating Driver	At Receiver
Differential “1”	(D+) - (D-) >200 mV and D+ or D- > Vse (min)	
Differential “0”	(D+) - (D-) < -200 mV and D+ or D- > Vse (min)	
Data (‘J’ State): Low Speed Full Speed	Differential “0” Differential “1”	
Data (‘K’ State): Low Speed Full Speed	Differential “1” Differential “0”	
Idle State: Low Speed Full Speed	Differential “0” and D- > VSE (max.) and D+ < VSE (min.) Differential “1” and D+ > VSE (max.) and D- < VSE (min.)	
Resume State: Low Speed Full Speed	Differential “1” and D+ > VSE (max.) and D- < VSE (min.) Differential “0” and D- > VSE (max.) and D+ < VSE (min.)	
Start of Packet (SOP)	Data lines switch from idle to ‘K’ State	
End of Packet (EOP)	D+ and D- < VSE (min) for 2 bit times1 followed by an Idle for 1 bit time	D+ and D- < VSE(min) for ≥ 1 bit time2 followed by a ‘J’ State
Disconnect (Upstream only)	(n.a.)	D+ and D- < VSE(max) for ≥ 2.5 µs
Connect (Upstream only)	(n.a.)	D+ or D- > VSE(max) for ≥ 2.5 µs
Reset (Downstream only)	D+ and D- < VSE for ≥10 ms	D+ and D- < VSE (min)for ≥ 2.5 µs (must be recognized by 5.5 µs)3

11.2 USB Physical Layer

Table 13. USB Physical Layer Specifications

Parameter	Symbol	Conditions	Min	Max	Unit
Supply Voltage:					
Powered (Host or Hub) Port	VBUS		4.75	5.25	V
Bus-powered Hub Port	VBUS		4.40	5.25	V
Supply Current:					
Powered Host/Hub Port (out)	ICCPRT		500		mA
Bus-powered Hub Port (out)	ICCUPT		100		mA
High Power Function (in)	ICCHPF			500	mA
Low Power Function (in)	ICCLPF			100	mA
Unconfig. Function / Hub (in)	ICCINIT			100	mA
Suspended Device	ICCS			500	µA
Leakage Current:					
Hi-Z State Data Line Leakage	ILO	0 V< VIN<3.3 V	-10	+10	µA
Input Levels:					
Differential Input Sensitivity	VDI	(D+)-(D-)	0.2		V
Differential Common Mode Range	VCM	Includes VDI range	0.8	2.5	V
Single Ended Receiver Threshold	VSE		0.8	2.0	V
Output Levels:					
Static Output Low	VOL	RL of 1.5 kΩ to 3.6 V		0.3	V
Static Output High	VOH	RL of 15 kΩ to GND	2.8	3.6	V
Capacitance:					
Transceiver Capacitance	CIN	Pin to GND		20	pF
Downstream Hub Port Bypass Capacitance	CHPB	Vbus to GND (Tantalum)	120		µF
Root Port Bypass Capacitance	CRPB	Vbus to GND Note 9	1.0	10.0	µF
Terminations:					
Bus Pull-up Resistor on Root Port	RPU	(1.5 kΩ ± 5%)	1.425	1.575	kΩ
Bus Pull-down Resistor on Down-stream Port	RPD	(15 kΩ ± 5%)	14.25	15.75	kΩ
Cable Impedance and Timing:					
Cable Impedance (Full Speed)	ZO	(45 Ω ±15%)	38.75	51.75	W

Table 13. USB Physical Layer Specifications (Continued)

Parameter	Symbol	Conditions	Min	Max	Unit
Cable Delay (one way)	TCBL			30	ns

NOTE:
1. Measured from 10% to 90% of the data signal.
2. Timing difference between the differential signals.
3. Measured at 50% swing point of data signals.
4. Load is RL on each output = 1.3 kΩ to 2.7 V and CL = 50 pF to GND
5. This is the voltage see at the receiver end of the cable immediately after a transition has occurred.
6. The maximum load specification is the maximum effective capacitive load allowed that meets the target hub VBUS drop of 330 mV.

Table 14. Full Speed Source Electrical Characteristics

Parameter	Symbol	Conditions	Min	Max	Unit
Driver Characteristics:					
Transition Time: Rise Time Fall Time	 TR TF	Note 5, 6 and CL = 50 pF CL = 50 pF	 4 4	 20 20	 ns ns
Rise / Fall Time Matching	TRFM	(TR/TF)	90	110	%
Output Signal Crossover Voltage	VCRS		1.3	2.0	V
Driver Output Resistance	ZDRV	Steady State Drive	28	43	W
Data Source Timings:					
Full Speed Data Rate	TDRATE	Ave. Bit Rate (12Mb/s ± 0.25%)	11.97	12.03	Mbs
Frame Interval	TFRAME	1.0 ms ± 0.05%	0.9995	1.0005	ms
Source Differential Driver Jitter To Next Transition For Paired Transitions	 TDJ1 TDJ2	Note 7, 8	 -3.5 -4.0	 3.5 4.0	 ns ns
Source EOP Width	TEOPT	Note 8	160	175	ns
Differential to EOP transition Skew	TDEOP	Note 8	-2	5	ns
Receiver Data Jitter Tolerance To Next Transition For Paired Transitions	 TJR1 TJR2	Note 8	 -18.5 -9	 18.5 9	 ns ns

Table 14. Full Speed Source Electrical Characteristics (Continued)

Parameter	Symbol	Conditions	Min	Max	Unit
EOP Width at receiver		Note 8			
Must reject as EOP	TEOPR1		40		ns
Must accept as EOP	TEOPR2		82		ns

NOTE:
1. All voltages measured from the local ground potential, unless otherwise specified.
2. All timings use a capacitive load (CL) to ground of 50 pF, unless otherwise specified.
3. Full Speed timings have a 1.5 kΩ pull-up to 2.8 V on the D+ data line.
4. Low Speed timings have a 1.5 kΩ pull-up to 2.8 V on the D- data line.
5. Measured from 10% to 90% of the data signal.
6. The rising and falling edges should be smoothly transitioning (monotonic).
7. Timing difference between the differential data signals.
8. Measured at crossover point of differential data signals.
9. The maximum load specification is the maximum effective capacitive load allowed that meets the target hub V_{BUS} drop of 330 mV.

Table 15. Low Speed Source Electrical Characteristics

Parameter	Symbol	Conditions	Min	Max	Unit
Driver Characteristics:					
Transition Time:		Note 5, 6			
Rise Time	TR	CL = 50 pF CL = 350 pF	75	 300	ns ns
Fall Time	TF	CL = 50 pF CL = 350 pF	75	 300	ns ns
Rise / Fall Time Matching	TRFM	(TR/TF)	80	120	%
Output Signal Crossover Voltage	VCRS		1.3	2.0	V
Data Source Timings:					
Low Speed Data Rate	TDRATE	Ave. Bit Rate (1.5Mb/s ± 1.5%)	1.4775	1.5225	Mbs

NOTE:
1. All voltages measured from the local ground potential, unless otherwise specified.
2. All timings use a capacitive load (CL) to ground of 50 pF, unless otherwise specified.
3. Full Speed timings have a 1.5 kΩ pull-up to 2.8 V on the D+ data line.
4. Low Speed timings have a 1.5 kΩ pull-up to 2.8 V on the D- data line.
5. Measured from 10% to 90% of the data signal.
6. The rising and falling edges should be smoothly transitioning (monotonic).
7. Timing difference between the differential data signals.
8. Measured at crossover point of differential data signals.
9. The maximum load specification is the maximum effective capacitive load allowed that meets the target hub V_{BUS} drop of 330 mV.

Table 15. Low Speed Source Electrical Characteristics (Continued)

Parameter	Symbol	Conditions	Min	Max	Unit
Source Differential Driver Jitter		Note 7, 8			
Host (Downstream):					
To Next Transition	TDDJ1		-75	75	ns
For Paired Transitions	TDDJ2		-45	45	ns
Function (Upstream):					
To Next Transition	TUDJ1		-95	95	ns
For Paired Transitions	TUDJ2		-150	150	ns
Source EOP Width	TEOPT	Note 8	1.25	1.50	µs
Differential to EOP transition Skew	TDEOP	Note 8	-40	100	ns
Receiver Data Jitter Tolerance		Note 8			
At Host (Upstream):					
To Next Transition	TUJR1		-152	152	ns
For Paired Transitions	TUJR2		-200	200	ns
At Function (Downstream):					
To Next Transition	TDJR1		-75	75	ns
For Paired Transitions	TDJR2		-45	45	ns
EOP Width at receiver		Note 8			
Must reject as EOP	TEOPR1		330		ns
Must accept	TEOPR2		675		ns

NOTE:
1. All voltages measured from the local ground potential, unless otherwise specified.
2. All timings use a capacitive load (CL) to ground of 50 pF, unless otherwise specified.
3. Full Speed timings have a 1.5 kΩ pull-up to 2.8 V on the D+ data line.
4. Low Speed timings have a 1.5 kΩ pull-up to 2.8 V on the D- data line.
5. Measured from 10% to 90% of the data signal.
6. The rising and falling edges should be smoothly transitioning (monotonic).
7. Timing difference between the differential data signals.
8. Measured at crossover point of differential data signals.
9. The maximum load specification is the maximum effective capacitive load allowed that meets the target hub V_{BUS} drop of 330 mV.

Table 16. Hub / Repeater Electrical Characteristics

Parameter	Symbol	Conditions	Min	Max	Unit
Hub Characteristics (Full Speed):					
Driver Characteristics (Refer to Table 7-5)		Root port and Downstream ports configured as Full Speed			
Hub Differential Data Delay		Note 3, 7, 8			
(with cable)	THDD1			70	ns
(without cable)	THDD2			40	ns
Hub Differential Driver Jitter (including cable)	THDJ1	Note 3, 7, 8	-3	3	ns
To Next Transition	THDJ2		-1	1	ns
For Paired Transitions					
Data bit width distortion after SOP	TSOP	Note 3, 8	-5	3	
Hub EOP Delay Relative to tHDD	TEOPD	Note 3, 8	0	15	ns
Hub EOP Output Width Skew	THESK	Note 3, 8	-15	15	ns
Hub Timings (Low Speed):					
Driver Characteristics (Refer to Table 7-6)		Downstream ports configured as Low Speed			
Hub Differential Data Delay	TLHDD	Note 4, 7, 8		300	ns
Hub Differential Driver Jitter (including cable)		Note 4, 7, 8			
Downstream:	TLDHJ1		-45	45	ns
To Next Transition	TLDHJ2		-15	15	ns
For Paired Transitions	TLUHJ1		-45	45	ns
Upstream:					
To Next Transition	TLUHJ2		-45	45	ns
For Paired Transitions					

NOTE:
1. All voltages measured from the local ground potential, unless otherwise specified.
2. All timings use a capacitive load (CL) to ground of 50 pF, unless otherwise specified.
3. Full Speed timings have a 1.5 kΩ pull-up to 2.8 V on the D+ data line.
4. Low Speed timings have a 1.5 kΩ pull-up to 2.8 V on the D- data line.
5. Measured from 10% to 90% of the data signal.
6. The rising and falling edges should be smoothly transitioning (monotonic).
7. Timing difference between the differential data signals.
8. Measured at crossover point of differential data signals.
9. The maximum load specification is the maximum effective capacitive load allowed that meets the target hub V_{BUS} drop of 330 mV.

Table 16. Hub / Repeater Electrical Characteristics (Continued)

Parameter	Symbol	Conditions	Min	Max	Unit
Data bit width distortion after SOP	TSOP	Note 4, 8	-60	45	
Hub EOP Delay Relative to tHDD	TLEOPD	Note 4, 8	0	200	ns
Hub EOP Output Width Skew	TLHESK	Note 4, 8	-300	+300	ns

NOTE:
1. All voltages measured from the local ground potential, unless otherwise specified.
2. All timings use a capacitive load (CL) to ground of 50 pF, unless otherwise specified.
3. Full Speed timings have a 1.5 kΩ pull-up to 2.8 V on the D+ data line.
4. Low Speed timings have a 1.5 kΩ pull-up to 2.8 V on the D- data line.
5. Measured from 10% to 90% of the data signal.
6. The rising and falling edges should be smoothly transitioning (monotonic).
7. Timing difference between the differential data signals.
8. Measured at crossover point of differential data signals.
9. The maximum load specification is the maximum effective capacitive load allowed that meets the target hub V_{BUS} drop of 330 mV.

12.0 DEVICE ERRATA

82930A devices with a topside FPO marking of Q8074 correctly address the following 256-Kbyte area of memory in Table 3, “82930A Memory Map”: 00:, 01:, FE:, and FF:. Designers should not use the following memory areas: 02:, 03:, FC:, and FD:. This is to be changed in future steppings of the 82930A.

13.0 REVISION HISTORY

The following information describes the differences between the first 82930A Product Preview datasheet (order number 272797-001) and this datasheet (order number 272797-002).

1. A more detailed 82930A block diagram appears in Figure 1.
2. Table 4, “68-lead Cerquad Signal Assignment Arranged by Functional Categories” contains corrected signal number references for ALE, PSEN#, EA#, and P3.6:7.
3. The T_{RHLH} minimum specification is modified.
4. The T_{WHLH} minimum specification is modified.
5. The T_{WHAX} minimum specification is modified.
6. The illustration for RD# and PSEN# non-page mode timing is now documented in separate illustrations. The new illustrations are Figure 5, “82930A Instruction Read, Non-page Mode” and Figure 6, “82930A Data Read, Non-page Mode”.
7. Configuration bits UCONFIG1.3 and UCONFIG1.0 are now reserved.
8. Table 12, “USB Signaling Levels” is revised to match Rev. 1.0 of the industry USB specification.
9. Table 13, “USB Physical Layer Specifications” is revised to match Rev. 1.0 of the industry USB specification.
10. Table 14, “Full Speed Source Electrical Characteristics” is new.
11. Table 15, “Low Speed Source Electrical Characteristics” is new.
12. Table 16, “Hub / Repeater Electrical Characteristics” is new.